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Analyzing the Impact of Process Variations at 32nm or below Process Nodes

Jaydeep Patel

Abstract— Process variation is the naturally occurring variation the attributes of transistors (length, widths, oxide thickness) when integrated circuits are fabricated. It becomes particularly important at 32nm or below process nodes as the variation becomes a larger percentage of the full length or width of the device. Thus, the design decisions based on the nominal models may not be correct because the models are either overestimations or underestimations of actual values; hence, the resultant circuits may not be optimal. Thus a number of Statistical Simulation Methodologies can be used to analyzing the impact of process variation on typical classes of circuits. The most common methodologies include (i) Monte Carlo (Full MC) (ii) Design of Experiment (Quasi MC) (iii) Most Probable Point (MPP). The Statistical Simulation techniques provide the greatest flexibility for studying the results of process variations. This allows process and device engineers to make realistic tradeoffs in setting process tolerances. This article analyzes impact of random delay variations on 5-stage CMOS inverter chain.

Index Terms— Process variation, Monte Carlo (Full MC), Design of Experiment (DOE), Most Probable Point (MPP).

1 INTRODUCTION

Moore's-Law-driven technology scaling has improved VLSI performance by five orders of magnitude in the last four decades. As advanced technologies continue the pursuit of Moore's Law, a variety of challenges will need to be overcome. One of these challenges is management of process variation [1, 2]. Although there has been a trend in the CMOS literature in recent years to convey process variation as a new challenge associated with advanced CMOS technologies, that viewpoint does not effectively capture the history of process variation. Process variation has always been a critical aspect of semiconductor fabrication.

Process variation is usually classified into two categories: die-to-die or inter-die, which is variation across different dies; and within-die or intra-die, which is variation among transistors within each die [3]. Die-to-die (D2D) variation changes the performance corner (fast or slow) of a particular die. The variation affects each transistor in the die in a systematic way; that is, if a die is in the high V_{th} (slow) corner, all transistors will have high V_{th}. On the other hand, within-die (WID) variation affects each transistor differently resulting in transistors with different V_{th} within close proximity due to effects such as random dopant fluctuations, line-edge roughness, or channel length variations. Increasing variations (both inter-die and intra-die) in device and interconnect parameters (channel length, gate width, oxide thickness, device threshold voltage etc.) produce large spread in the speed and power consumption of integrated circuits (ICs) [4]. Consequently, parametric yield of a circuit (probability to meet the desired performance or power specification) is expected to suffer.

1.1 Random Dopant Fluctuation (RDF)

MOS threshold voltage variation due to random fluctuations in the number and location of dopant atoms is an increasingly significant effect in sub-micron CMOS technologies (see Fig. 1 and [5]). As the number of dopant atoms in the channel decreases with scaled dimensions, the impact of the variation associated with the atoms increases. Fig. 2 illustrates the decreasing average number of dopant atoms in the channel as a function of the technology node [5]. Note the change from the 1µm technology node (with many thousands of dopant atoms in the channel) to the 32nm technology node (with less than 100 atoms in the channel).

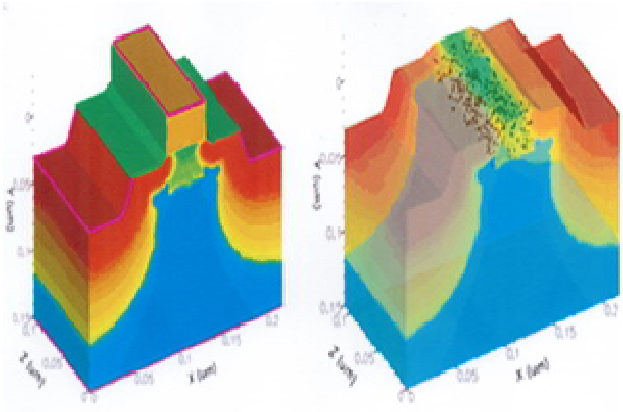

Fig. 1. Random dopant fluctuations (RDF) are an important effect in sub-micron CMOS technologies.

RDF is assumed to be the major contributor to device mismatch of identical adjacent devices and is frequently represented by Stolk's formulation (Equation 1)

$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^2\varepsilon_{si}\phi_B}}{2}\right).\frac{T_{ox}}{\varepsilon_{ox}}.\left(\frac{\sqrt[4]{N}}{\sqrt{W_{eff}.L_{eff}}}\right) = \frac{1}{\sqrt{2}}\left(\frac{C_2}{\sqrt{W_{eff}.L_{eff}}}\right) \quad (1)$$

illustrating that matching improves with decreases in channel doping (N) and gate oxide thickness (T_{ox}), and it degrades when device area decreases [6].

Jaydeep Patel is currently pursuing masters degree program in VLSI Design in Nirma University, Ahmedabad, India. E-mail: jaydeep2488@gmail.com

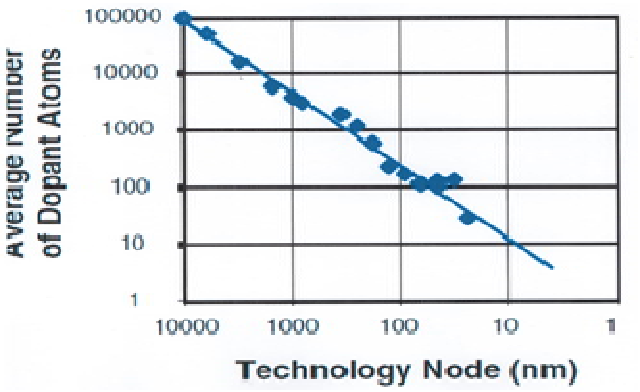

Fig. 2. Average number of dopant atoms in the channel as a function of technology node.

2 Statistical Simulation Methodologies

Statistical Simulation helps a circuit designer to determine which transistors in a circuit are most influential on its performance and how variations of the device and process parameters affect the circuit output responses.

2.1 Monte Carlo (Full MC)

The most common statistical simulation method is Monte-Carlo (MC) [7]. It is based on multiple simulations using random sampling (Fig. 3) of the variables. This is a general method in the sense that it can be applied without previous assumptions on the function behavior. In theory, MC can achieve as much accuracy as desired at the cost of simulation time. In practice, the required simulation time may be prohibitive. The main weakness of this method is the excessive number of simulations that produce redundant information. In MC number of splits depends on the variation sigma. Basically we used 500-1000 simulations for 3σ output spec.

2.2 Design of Experiment (Quasi MC)

For certain class of circuits, if we need to target 4σ or above, then Monte Carlo won't be a viable solution as it would require more than 10000 simulations and this could be resource intensive and time consuming. To solve this problem, we explored the DOE/RSM based statistical simulation method as this requires lesser number of simulations to achieve the same. Special designed points (Fig. 4 and [8]) are selected in the parameter space using DOE methods as experiments (splits). The Screening designs are used to screen out less important process factors and reduce number of simulations. To model the impact of multiple process variations on circuits, Design of Experiments (DOE) is performed and second order models are built using Response Surface Model (RSM) [8]. Models obtained, using simulation data, are polynomials of the form

$$y = C_0 + C_1 X_1 + C_{11} X^2 + \cdots$$

Here C_0 is nominal value.

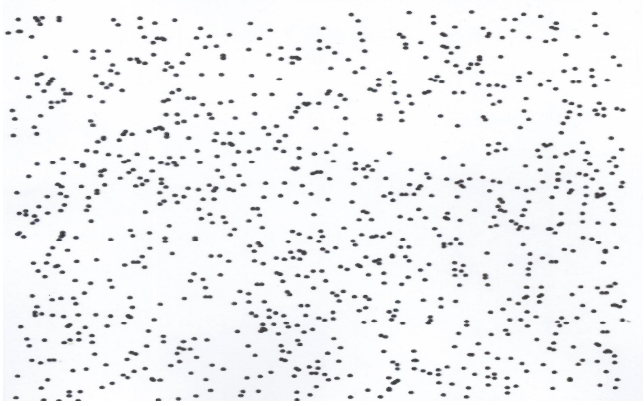

Fig. 3. Drawing random sample from design space.

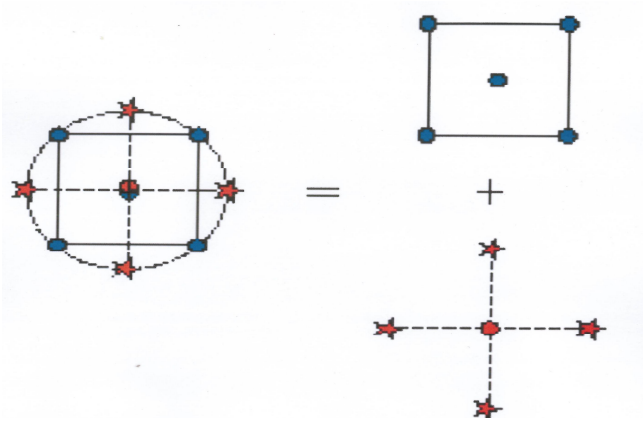

Fig. 4. DOE for 2nd order polynomial fitting.

2.3 Most Probable Point (MPP)

If we need target on 5σ or above, then Monte Carlo and Design of Experiment methods are failed. So, we explored the Most Probable Point (MPP) statistical simulation method to meet 5σ output spec. MPP is an algorithmic approach to solve for the Nσ variation point of the response directly. For a predefined specific distance, the failure surface can be searched such that the minimum distance from the surface to origin is equal to that specified distance (Fig. 5 and [9]). MPP commonly used for circuits that require validation at higher sigma.

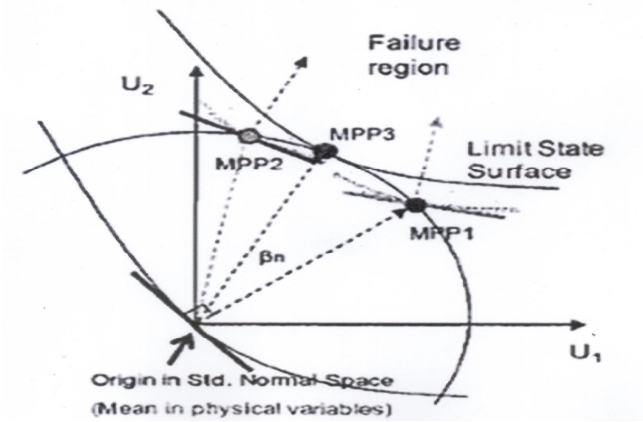

Fig. 5. Searching MPP on a specified β (probability level).

3 SIMULATION RESULTS

In this paper we are simulated 5-stage CMOS inverter chain circuit (Fig. 6) at RSSS process corner, 0.95V supply voltage, and 125C temperature. We measured rise to fall (RF) delay at output stage. We ran MC and DOE simulations in order to randomly vary threshold voltage (V_{th})(Eqn. 1) and gate length (L_g) values of each transistor based on a Gaussian distribution with an assigned mean (μ) and standard deviation (σ) shown in Table I. From mean and sigma we could calculate output target spec using μ±Nσ, where N = 1, 2…6.

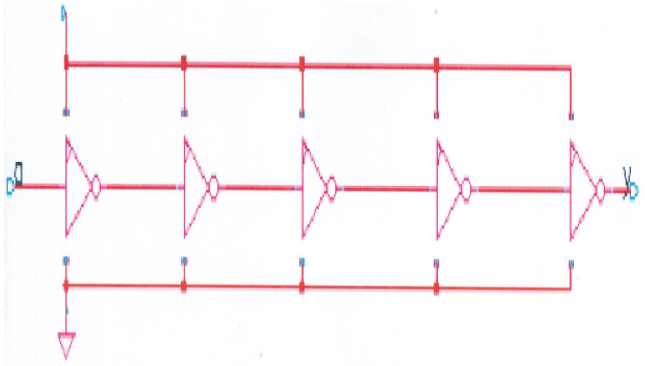

Fig. 6. Schematic of 5-stage inverter chain.

TABLE I. 5-stage CMOS inverter chain MC & DOE Results

Methods	RF delay (ps)						
	Nominal	*mean*	*sigma*	*3σ*	*4σ*	*5σ*	*6σ*
MC	56.6548	56.8467	3.8089	68.2734	72.0823	75.8912	79.7001
DOE	56.6548	57.0149	3.8240	68.48708	72.31114	76.1352	79.95926

Variations due to the MC and DOE (Quasi MC) analysis assign each transistor V_{th} and L_g deviating from its original value based on the input we assigned. Basically we used 800 simulations as an input for 3σ output spec in MC and 3σ variations as an input in DOE. This cause inverter chain rise to fall delay either be higher or lower than the expected value because variations may either improve or degrade the delay (Fig. 7).

Fig. 8 shows the results of MC 800 simulations of last stage inverter chain output. From the simulation results we can see that simulation tool generate 800 different splits according to selecting random (V_{th}, L_g) point from design space and simulate 800 different delay outputs.

Fig. 9 (a) and (b) show the quantile plot of MC and DOE respectively. From a point (x, y) on the plot we could find sigma corresponds to delay or vice versa. From Fig.8 we conclude that 800 simulations requirement for MC to achieve 3σ output spec and DOE (Quasi MC) method used for 4σ or above target.

In DOE a Response Surface Model (RSM) experiment tries to fit a data value to the variables of the experiment using a polynomial function. In this paper, the polynomial is at most quadric. Fig. 10 shows that measured simulation results RF delay (x-axis) versus responses evaluated from RSM. If the RSM fit is perfect, the points will fall along a 45-degree straight line. We target R^2 (coefficient of determination) > 0.99 indicates that a regression line fits the data well.

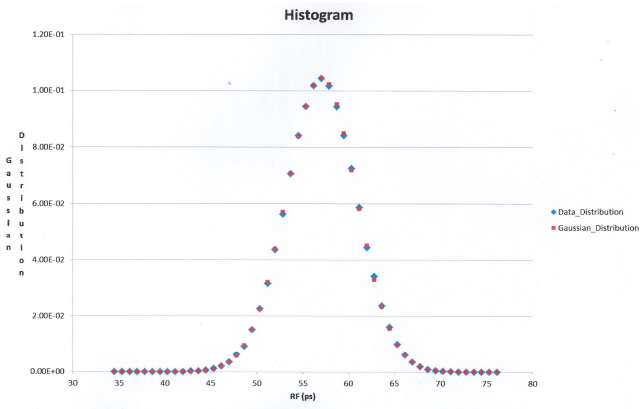

Fig. 7. Delay distribution of 5-stage inverter chain.

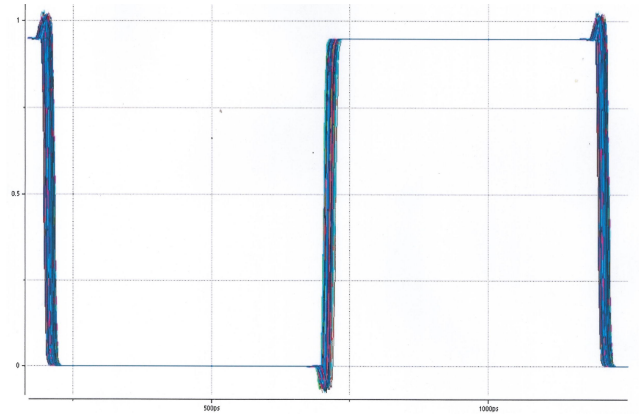

Fig. 8. MC 800 simulations of 5-stage inverter chain output.

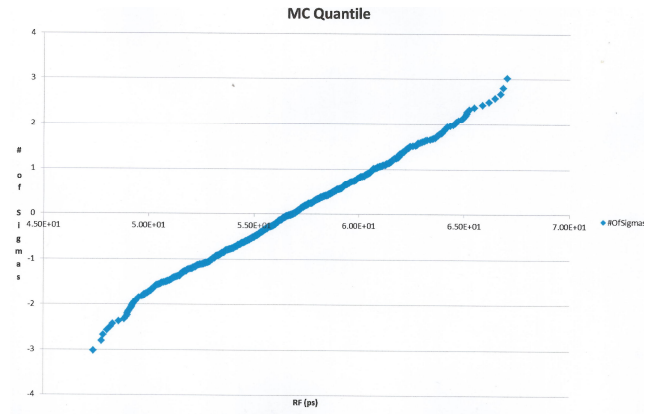

Fig. 9 (a). MC Quantile Plot.

The results of MPP experiment are displayed in Fig. 11. MPP finds the circuit response (delay) associated with each requested higher sigma. At present MPP is the more robust algorithm. MPP constraint the variation amount (ns sphere) and find the worst variation point (largest RF delay). Since it's an iterative process, it requires much more time to simulate. Thus for highly linear behavior, it's better to use the DOE approach.

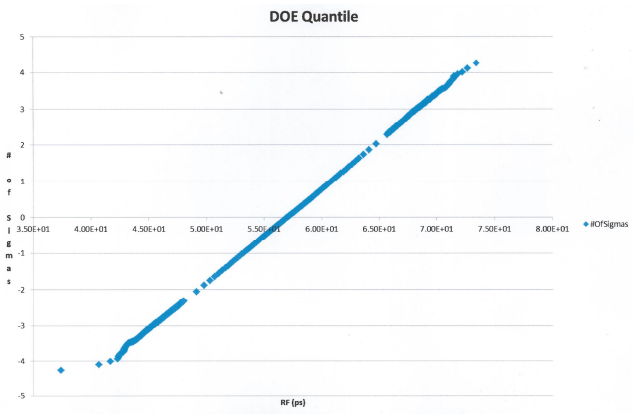

Fig. 9 (b). DOE Quantile Plot.

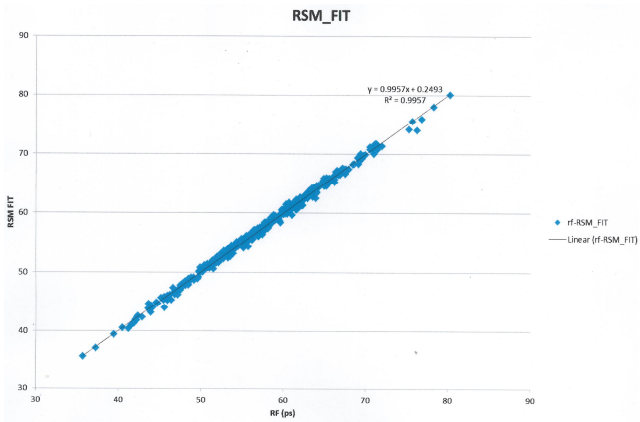

Fig. 10. Delay vs. RSM FIT.

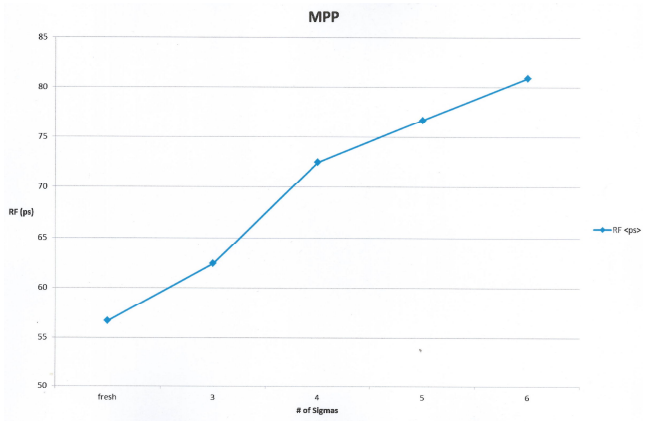

Fig. 11. MPP results of 5-stage inverter chain.

4 Conclusion

We presented in this paper an analysis of process variations on 5-stage inverter chain. The effect of process variability has become a critical issue at 32nm or below process nodes. An in-depth study of the effect of process variability is thus essential for robust designing of a nano-scale CMOS circuits. With process variation, the variation in performances is found to be Gaussian in nature. The spread of performances is found to be significant compared to the mean value of the performances. According to the output target spec the statistical simulation methodologies on 32nm or below technologies were performed and validate the analysis developed.

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